In re Patent Application of:
OM ET AL.
Serial No. **10/806,938**
Filing Date: **March 23, 2004**

REMARKS

The Examiner is thanked for the thorough examination of the present application and for the Examiner interview of September 14, 2005. During the interview, the Examiner clarified that the independent claims were rejected based upon the Frane patent and not the Feldman patent as indicated in the rejection.

Independent Claims 1, 6, 11, and 16 have been amended to more clearly define the subject matter over the prior art. In addition, Claims 1 and 6 were also amended to correct minor informalities using the Examiner's helpful suggestions. Accordingly, the objections to Claim 1 and 6 are overcome.

The patentability of the claims is discussed in greater detail below. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

Amended independent Claim 6, for example, is directed to a digital logic system comprising a reset input for receiving a reset signal, a clock input for receiving an externally generated main clock signal, and an ancillary clock generator for generating an ancillary clock signal independent of the externally generated main clock signal. The digital logic system also comprises a clock selection multiplexer having a first input for receiving the externally generated main clock signal, a second input for receiving the ancillary clock signal, and an output for providing the externally generated main clock signal or the ancillary clock signal. The digital logic system further comprises a shift register

having a first input for receiving the externally generated main clock signal, a second input for receiving the reset signal, and an output connected to the clock selection multiplexer for deselecting the ancillary clock signal and selecting the externally generated main clock signal after detecting a certain number of edges of the main clock signal following the reset signal. Amended independent Claim 16 is a method counterpart to Claim 6 and includes similar recitations.

Amended independent Claim 11 is similar to Claim 6 and further recites a functional circuit. Amended independent Claim 1 is similar to Claim 11 further recites and that the ancillary clock signal has short term frequency stability in relation to an expected duration of a system reset phase.

II. All The Claims Are Patentable

The Examiner rejected independent Claims 1, 6, 11, and 16 as unpatentable over the Frane patent. The Frane patent discloses a clock generator 132 for generating a clock signal that is transmitted to a divider circuit 140 as is described at column 3, lines 8-16 and in FIG. 1. In other words, the clock signal derived by the divider circuit 140 is based upon the clock signal of the clock generator 132.

In contrast, amended independent Claim 6, for example, is directed to a digital logic system comprising a clock input for receiving an externally generated main clock signal, and an ancillary clock generator for generating an ancillary clock signal independent of the externally generated main clock signal. The digital logic system further comprises a shift register having a first input for receiving the

externally generated main clock signal, a second input for receiving a reset signal, and an output connected to a clock selection multiplexer for deselecting the ancillary clock signal and selecting the externally generated main clock signal after detecting a certain number of edges of the main clock signal following the reset signal.

The Frane patent fails to disclose an ancillary clock generator for generating an ancillary clock signal independent of the externally generated main clock signal. For example, the loss of the Frane clock generator 132 would prevent the divider circuit 140 from providing any output due to the absence of the clock generator's clock signals. In comparison, the claimed ancillary clock generator can generate an ancillary clock signal even when the main clock signal is lost.

The Frane patent also fails to disclose a shift register having an output connected to a clock selection multiplexer for deselecting the ancillary clock signal and selecting the externally generated main clock signal after detecting a certain number of edges of the main clock signal following the reset signal. Instead the Frane patent discloses that the clock generator 132 is selected based upon the clock disable signal 150 rather than after detection of a certain number of edges of the main clock signal following a reset signal. Amended independent Claims 1, 11, and 16 recite recitations similar to Claim 6.

Accordingly, amended independent Claims 1, 6, 11, and 16 are patentable. The dependent claims, which recite yet further distinguishing features of the invention, are also patentable, and require no further discussion.

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CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 14th day of October, 2005.